A THEORY FOR THE PREDICTION OF GaAS FET LOAD-PULL POWER CONTOURS

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ABSTRACT

A theory is presented which is capable of predicting the power load-pull contours of a GaAs FET in a convenient mathematical formulation. Although based on some initial simplifying assumptions, the predicted contours are shown to be in good agreement with experimental measurements.

Introduction

The use of load-pull contours in the design of solid state power amplifiers is now well established. The information contained in a load-pull plot is of particular importance for broader band designs, where exact synthesis of the optimum output load at all frequencies is not possible and a compromise must be made. Unfortunately, the generation of a set of load-pull contours is a laborious procedure if performed manually using mechanical tuners. As a result, several workers have built computer controlled systems which undoubtedly speed up the measurement procedure but involve a large capital expenditure in dedicated equipment and setting-up time which cannot always be justified. Additionally, the accuracy of such systems, which ultimately rely on the resettability and loss calibration of a mechanical tuner, must come into question at higher microwave frequencies. What the broadband power designer really needs is a simple mathematical formulation from which contours of constant power on a Smith chart can be generated at will, in an analogous manner to the noise circles used for the design of low noise amplifiers. The problem is that the experimentally generated contours are clearly not circles, and it has always been assumed that any theory that will predict such contours must inevitably take account of the non-linear behaviour of the device as it is driven into saturation. This paper presents a theory which is capable of predicting load-pull contours with good accuracy but which is based on simple linear circuit concepts.

The Linear Approximation

Figure 1 shows a typical input/output power characteristic of a medium power GaAs FET (Watkins-Johnson F2710R). When tuned for maximum small signal gain (dotted curve) the device saturates at an output power level typically 2-3dB lower than when tuned for optimum power (solid curve). A highly significant observation from these familiar curves is that the power improvement in going from small signal to optimum power tuning is much the same whether the criterion is based on saturated power (points C and C') or the 1dB compression power (points B and B') or the maximum linear power (points A and A'). The immediate implication of this, which can be confirmed by more extensive measurements, is that the output load required for maximum saturated power is very nearly the same as the load required either for optimum 1dB compression power or maximum linear power. If, therefore, a theory is developed which predicts the power versus output load behaviour in the relatively straightforward linear case, the results can be used with confidence to predict the behaviour in the non-linear regime.

Figure 2 shows an idealised model of a linear FET amplifier. The device is represented as a current generator which swings linearly from zero to I_{DSS} with varying input gate voltage. Assuming that the R. F. load and D. C. biasing elements are suitably separated, the R. F. voltage at the drain can swing to a maximum value of 2 V_{DSS}. It is an elementary and well known result that for maximum linear power the R. F. load must be resistive and given by:

$$R_{OPT} = V_{DSS} / \tfrac{1}{2} I_{DSS} \quad \ldots\ldots (1)$$

This simple result is widely used as a design parameter for linear amplifiers at lower frequencies. At microwave frequencies, impedance measurements become increasingly dominated by device and package reactances which distort the simple picture. However, detailed measurements on medium and higher power GaAs FETs show that provided the FET drain capacitance is de-embedded as part of the external outputload, the optimum output impedance is indeed still resistive, and is close to the low-frequency value given in (1). Figure 2 shows a plot of measured values of optimim load resistance for a wide range of GaAs FET types from which it can be seen that they fall closely on the line representing the ideal linear model.

Power Variation with Load

Having established that the simple linear model of Figure 3 can predict the output load for optimum power with useful accuracy, the concept can be taken one step further by considering the values of maximum linear power predicted for any general output load Z_L. This will then lead directly to a load-pull contour plot.

In general, if the modulus of the output load Z_L is less than Ropt, linear operation is fundamentally limited by the maximum available current swing I_{DSS}. If Z_L is greater than Ropt, the maximum voltage swing 2 V_{DSS} is the constraint. It is convenient to consider these two cases separately (Figure 4).

(i) Z1 Ropt

In this case it is most convenient to consider the Load Z_L as a series connection of its resistive and reactive components, i.e. $Z_L = R_L + jX_L$. Clearly, the maximum linear power for this load, P1, is given by:

$$P_L = \left[\tfrac{1}{2} I_{DSS}\right]^2 . R_L$$

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or, normalizing in terms of the optimum power Popt and the optimum load Ropt:

$$\frac{P_L}{P_{OPT}} = \frac{R_L}{R_{OPT}} \quad \ldots\ldots\ldots (2)$$

The instantaneous drain voltage is given by:

$$V_L = I_D(T) . Z_L$$

Whence

$$\hat{V}_L = I_{DSS}\sqrt{(R_L^2 + X_L^2)}$$

Substituting for I_{DSS} from (1):

$$\hat{V}_L = \frac{2V_{DSS}}{R_{OPT}}\sqrt{(R_L^2 + X_L^2)} \quad \ldots\ldots (3)$$

Thus, in order to keep the voltage swing less than the maximum permissible value of 2 V_{DSS}, Xl can take any positive or negative value up to a maximum given by:

$$|X_L|^2 \leq (R_{OPT}^2 - R_L^2) \quad \ldots\ldots\ldots (4)$$

(ii) Z1 Ropt

In this case Z1 is most conveniently considered as a parallel connection of its conductive and susceptive components, i.e. $Y_L = G_L + jB_L$. The maximum linear power is given by

$$P_L = \left[\tfrac{1}{2}V_{DSS}\right]^2 . G_L$$

i.e.

$$\frac{P_L}{P_{OPT}} = \frac{G_L}{G_{OPT}} \quad \ldots\ldots\ldots (5)$$

By analagous reasoning to case (i), it can be shown that the power is constant for values of susceptance within the limits

$$|B_L|^2 \leq (G_{OPT}^2 - G_L^2) \quad \ldots\ldots\ldots (6)$$

Construction of Load-Pull Contours

Equations (1) through (6) supply all the information needed to construct a load-pull contour, for a given power P . As an example, consider a typical 1 Watt GaAs FET device with I_{DSS} of 0.6A operating at a V_{DSS} of 10V. From (1) Ropt = 33.3 ohms. A 1dB power contour can be constructed around this optimum point as follows:

(a) The two resistive points on the contour can be obtained directly from (2) and (5), in this case these values are 42ohms and 26.5 ohms.

(b) Starting at the lower resistance point in (a) the contour follows the constant resistance line on the Smith chart, up to the reactance limits given in (4).

(c) Starting at the higher resistance point in (a) the contour follows the constant conductance line on the Smith chart, up to the susceptance limits given in (6).

Figure 5 shows the result for both 1dB and 2dB power contours. It should be noted that the two sections of the contour described in (b) and (c) above always intersect at the limiting values given in (4) and (6) and it is not necessary to evaluate these limits in order to construct the contours on a Smith chart.

Comparison with Measured Load-Pull Contours

The contours in Figure 5a assume that the drain capacitance and bondwire/package reactances are absorbed in the external load. In order to compare these results with experimental measurements, it is more convenient to add in the drain capacitance and bondwire inductance (0.6pF and 0.3nH respectively, values taken from small-signal measurements) to the theoretical plots. This results in the significantly modified contour shapes shown in Figure 5b. An experimental plot for a device of this type is shown in Figure 6. The agreement is good and may be within the experimental error limits of the measurements. From a design point of view, it would appear that the theoretical contours are more pessimistic in terms of power than the measured ones and therefore represent a good target for broadband design.

Conclusion

A theory has been developed which can predict the optimum output load and load-pull contours for a power GaAs FET. The load-pull contours can be generated from simple mathematical expressions which may be readily incorporated into CAD programs. The theory is based on simple linear circuit concepts, but has been shown to give close agreement with experimental measurements.

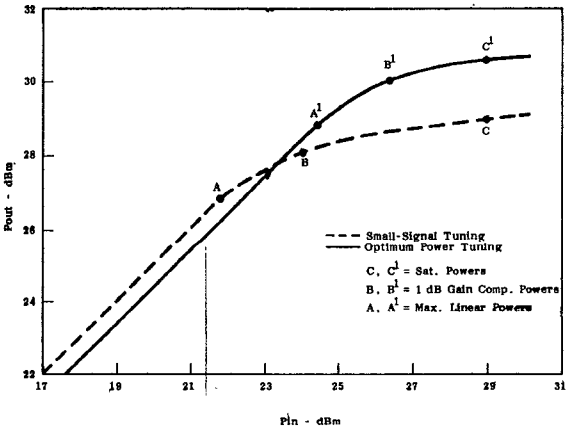


Figure 1: Power FET Input/Output Characteristics

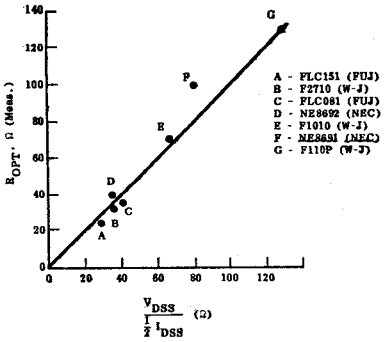


Figure 2: Measured Values of R_{OPT} vs. Theoretical Prediction

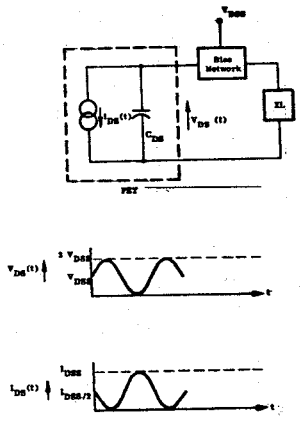


Figure 3: Linear FET Model

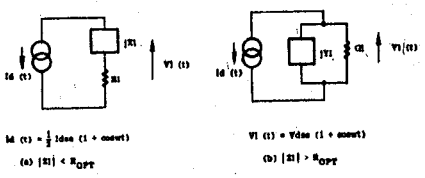
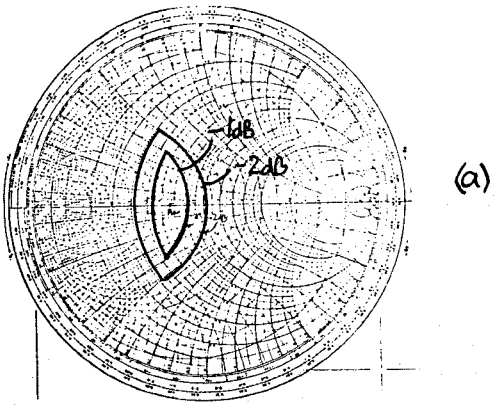


Figure 4: Equivalent Circuits for General Drain Load Analysis



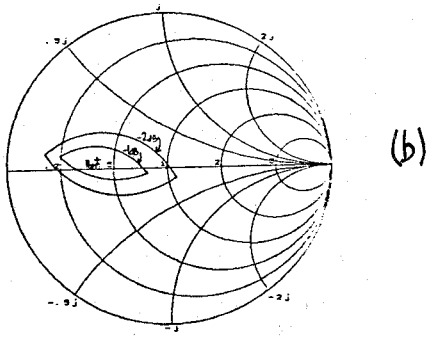


Fig. 5 Theoretical Output Load-pull Contours for 1 Watt GaAsFET.

(a) Drain capacitance and bondwire inductance treated as part of external load
(b) Same as (a) but reference plane shifted to outside drain bondwire

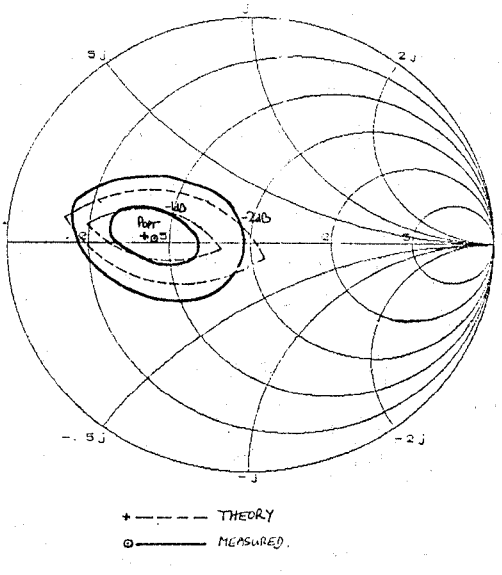


Fig. 6 Comparison of predicted and measured output load-pull contours for a 1 Watt GaAsFET (F2710, 8 GHz)